INEXPENSIVE WAFER LEVEL MMIC CHIP PACKAGING

ABSTRACT OF THE DISCLOSURE

An inexpensive package for a semiconductor chip (1) that incorporates a stress relief buffer (13) between a side of the chip and the metal carrier layer (2) to absorb thermally induced stress produced by significantly different rates of thermal expansion of the wafer and the metal carrier. The buffer (13) is formed by a polymer that is flexible and can be etched, contains a coefficient of thermal expansion that does not significantly differ from that of the chip and/or a combination of CET and elasticity that retains a physical connection with the side of the chip and the metal carrier over the temperature range of operation anticipated for the chip. Polyimide or paraylene are preferred examples. Vias (15) extend through the buffer to place the metal carrier electrically in common with the metal layer (5) found on the back surface of the wafer so that an electrical ground applied to the metal carrier layer (2) may extend through to that surface.